WE CLAIM:

1. A printed wiring board (PWB) for mounting a high performance ball grid array (BGA) device on one side of said PWB, comprising:

a modified vias array, the modification being that at least a portion of one row of said vias array is missing at least two adjacent vias, wherein the missing vias have been replaced by respective shared vias in an adjacent row, and said shared vias have been connected to either a power supply or a power return; and

a via pad for each said shared vias located on the other side of said PWB in said portion,

whereby a decoupling capacitor can be electrically connected across said pair of via pads to decouple the power supply and the power return at said two adjacent vias.

2. A printed wiring board (PWB) for mounting a high performance integrated circuit, comprising:

on a top side of said PWB, a modified via array with BGA columns and BGA rows of ball connection pads;

a modified vias array of plated through hole (PTH) vias, with each via column Col(n) arranged between two respective BGA columns c(n) and c(n+1) and each via row R(k) arranged between two respective BGA rows r(k) and r(k+1),

wherein 2m vias of said via column Col(n) placed in successive via rows R(k) to R(k+2m-1) of said modified vias array are depopulated to obtain a free space on the back side of said PWB, and

wherein 2m corresponding vias in a via column C(n+1) adjacent to said column Col(n) and placed in said successive rows R(k) to R(k+2m-1) of said vias array are shared vias.

3. The PWB of claim 2, wherein said free space has a width D1 equal to twice the pitch D of said vias array less a via size, for accommodating m passive elements of a substantially similar width D1.

4. The PWB of claim 2, wherein m is at least one.

5. The PWB of claim 2, wherein a first shared via in said column Col(n) and said row R(k) provides a power contact to a first associated ball contact pad in said column c(n) and said row r(k) and to a second associated ball contact pad in said column c(n+1) and said row r(k).

6. The PWB of claim 5, wherein a second shared via in said column Col(n) and said row R(k+1) provides a ground contact to a third associated ball contact pad in said column c(n) and said row r(k+1) and to a fourth associated ball contact pad in said column c(n+1) and said row r(k).

7. The PWB of claim 2, wherein a first shared via in said column Col(n) and said row R(k) provides a power contact to a first associated ball contact pad in said column c(n) and said row r(k) and to a second associated ball contact pad in said column c(n+1) and said row r(k+1).

8. The PWB of claim 7, wherein a second shared via in said column Col(n) and said row R(k+1) provides a ground contact to a third associated ball contact pad in said c(n) and said row r(k+1) and to a fourth associated ball contact pad in said column c(n+1) and a row r(k+2).

9. The PWB of claim 2, wherein a first shared via in said column Col(n) and said row R(k) provides a power contact to a first associated ball contact pad in said column c(n) and said row r(k+1) and to a second associated ball contact pad in said column c(n+1) and said row r(k).

10. The PWB of claim 9, wherein a second shared via in said column Col(n) and said row R(k+1) provides a ground contact to a third associated ball

contact pad in said c(n) and said row r(k+2) and to a fourth associated ball contact pad in said column c(n+1) and a row r(k+1).

11. The PWB of claim 3, wherein said passive elements are 0603, 0402, 0201 or smaller decoupling capacitors.

12. The PWB of claim 3, wherein said passive elements are 0603, 0402, 0201 or smaller resistors.

13. For a printed wiring board (PWB) having a land pattern for mounting a BGA device on one side of said PWB and a vias array for connecting said BGA device to said PWB a method for mounting a decoupling capacitor on the other side of said PWB, comprising:

depopulating at least two adjacent vias in a portion of a first row of said vias array;

replacing said depopulated vias by a pair of shared vias in a second row, adjacent to said first row;

connecting said shared vias to a power supply and a power return respectively and providing a respective via pad for said shared vias on the other side of said PWB in said portion; and

electrically connecting said decoupling capacitor across said pair of shared vias to decouple the power supply and the power return at said two adjacent vias.